Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **A**
2. **B**
3. **J**
4. **K**
5. **C**
6. **D**
7. **VSS**
8. **E**
9. **F**
10. **L**
11. **M**
12. **G**
13. **H**
14. **VDD**

**.057”**

**.040”**

**DIE ID**

**6 7 8**

**1 14 13**

**12**

**11**

**10**

**9**

**2**

**3**

**4**

**5**

**CD**

**4011B**

**J = A.B**

**K = C.D**

**L = E.F**

**M = G.H**

**Top Material: Al**

**Backside Material: Si Ni**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4011B**

**APPROVED BY: DK DIE SIZE .040” X .057” DATE: 6/22/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: CD4011BH**

**DG 10.1.2**

#### Rev B, 7/19/02